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[DYNAMIC RANDOM ACCESS MEMORY CELL AND FABRICATION THEREOF]

Abstract

A dynamic random access memory (DRAM) cell is described, including a semiconductor pillar on a substrate, a capacitor on a lower portion of a sidewall of the pillar, and a vertical transistor on an upper portion of the sidewall of the pillar. The vertical transistor includes a first doped region, a second doped region, a gate and a gate insulating layer. The first doped region is located in the sidewall and is coupled with the capacitor. The second doped region is located in a top portion of the pillar. The gate is disposed on the sidewall of the pillar between the first and the second doped regions, and the gate insulating layer is disposed between the sidewall and the gate.